WHAT IS CLAIMED IS:

1. An integrated circuit (IC) device outputs test protection circuit comprising:

decision circuitry responsive to predetermined boundary scan register (BSR) signals and a test access port (TAP) controller mode signal to generate a first logic signal;

a test protection circuit register responsive to the first logic signal, a test clock and a TAP controller instruction to generate a second logic signal; and

logic circuitry responsive to at least one BSR signal and the second logic signal to generate a protection circuit output control signal, wherein the protection circuit output control signal operates within one test clock cycle to disable an output buffer associated with a short circuit corresponding to the IC device.

2. The IC device outputs test protection circuit according to claim 1, wherein the predetermined BSR signals comprise a primary input buffer signal, an output BSR signal and a control BSR update register control signal.

3. The IC device outputs test protection circuit according to claim 2, wherein the decision circuitry comprises exclusive OR circuitry operational to receive the primary input buffer signal and the output BSR signal.

4. The IC device outputs test protection circuit according to claim 1, wherein the test protection circuit register is further responsive to a previous protection data register (DR) associated with a corresponding protection DR chain to generate the second logic signal.

5. An integrated circuit (IC) device outputs test protection circuit comprising:

means responsive to predetermined boundary scan register (BSR) signals and a test access port (TAP) controller mode signal for generating a first logic signal;

means responsive to the first logic signal, a test clock and a TAP controller instruction for generating a second logic signal; and

means responsive to at least one BSR signal and the second logic signal for generating a protection circuit output control signal, wherein the protection circuit output control signal operates within one test clock cycle to disable an output buffer associated with a short circuit corresponding to the IC device.

6. The IC device outputs test protection circuit according to claim 5, wherein the means for generating a first logic signal comprises decision circuitry.

7. The IC device outputs test protection circuit according to claim 5, wherein the means for generating a second logic signal comprises a test protection circuit register.

8. The IC device outputs test protection circuit according to claim 7, wherein the test protection circuit register is further responsive to a previous protection data register (DR) associated with a corresponding protection DR chain to generate the second logic signal.

9. The IC device outputs test protection circuit according to claim 5, wherein the means for generating a protection circuit output control signal comprises logic circuitry.

10. The IC device outputs test protection circuit according to claim 5, wherein the predetermined BSR signals comprise a primary input buffer signal, an output BSR signal and a control BSR update register control signal.

11. The IC device outputs test protection circuit according to claim 10, wherein the means for generating a first logic signal comprises exclusive OR circuitry operational to receive the primary input buffer signal and the output BSR signal.

12. A protection circuit operational to prevent damage to a good device during JTAG final testing of a circuit board that employs the good device.

13. The protection circuit according to claim 12, comprising logic circuitry responsive to predetermined BSR signals to generate a protection circuit output control signal that operates within one test clock cycle to disable an output buffer associated with a short circuit or overload condition corresponding to the good device.

14. The protection circuit according to claim 13, wherein the predetermined BSR signals comprise a primary input buffer signal, an output BSR signal and a control BSR update register control signal.

15. The protection circuit according to claim 12, comprising:

decision circuitry responsive to predetermined boundary scan register (BSR) signals and a test access port (TAP) controller mode signal to generate a first logic signal;

a test protection circuit register responsive to the first logic signal, a test clock and a TAP controller instruction to generate a second logic signal; and

logic circuitry responsive to at least one BSR signal and the second logic signal to generate a protection circuit output control signal, wherein the protection circuit output control signal operates within one test clock cycle to disable an output buffer associated with a short circuit corresponding to the IC device.

16. The protection circuit according to claim 15, wherein the predetermined BSR signals comprise a primary input buffer signal, an output BSR signal and a control BSR update register control signal.

17. The protection circuit according to claim 16, wherein the decision circuitry comprises exclusive OR circuitry operational to receive the primary input buffer signal and the output BSR signal.

18. The protection circuit according to claim 15, wherein the protection circuit register is further responsive to a previous protection data register (DR) associated with a corresponding protection DR chain to generate the second logic signal.

19. The protection circuit according to claim 12, comprising:

means responsive to predetermined boundary scan register (BSR) signals and a test access port (TAP) controller mode signal for generating a first logic signal;

means responsive to the first logic signal, a test clock and a TAP controller instruction for generating a second logic signal; and

means responsive to at least one BSR signal and the second logic signal for generating a protection circuit output control signal, wherein the protection circuit output control signal operates within one test clock cycle to disable an output buffer associated with a short circuit corresponding to the IC device.

20. The IC device outputs test protection circuit according to claim 19, wherein the means for generating a first logic signal comprises decision circuitry.

21. The IC device outputs test protection circuit according to claim 19, wherein the means for generating a second logic signal comprises a test protection circuit register.

22. The IC device outputs test protection circuit according to claim 21, wherein the test protection circuit register is further responsive to a previous protection data register (DR) associated with a corresponding protection DR chain to generate the second logic signal.

23. The IC device outputs test protection circuit according to claim 19, wherein the means for generating a protection circuit output control signal comprises logic circuitry.

24. The IC device outputs test protection circuit according to claim 19, wherein the predetermined BSR signals comprise a primary input buffer signal, an output BSR signal and a control BSR update register control signal.

25. The IC device outputs test protection circuit according to claim 24, wherein the means for generating a first logic signal comprises exclusive OR circuitry operational to receive the primary input buffer signal and the output BSR signal.

26. A method of providing integrated circuit (IC) device outputs protection during JTAG board tests, the method comprising the steps of:

providing an IC device outputs test protection circuit including decision circuitry responsive to predetermined boundary scan register (BSR) signals and a test access port (TAP) controller mode signal to generate a first logic signal; a test protection circuit register responsive to the first logic signal, a test clock and a TAP controller instruction to generate a second logic signal; and logic circuitry responsive to at least one BSR signal and the second logic signal to generate a protection circuit output control signal; and

generating the protection circuit output control signal within one test clock cycle to disable an output buffer associated with a short circuit condition or overload condition corresponding to an IC device.